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Veronica Rispo

WORK EXPERIENCE

01/10/2023 – CURRENT Pisa, Italy
PH.D STUDENT IN EMERGING DIGITAL TECHNOLOGIES - CURRICULUM EMBEDDED SYSTEMS
SCUOLA SUPERIORE SANT'ANNA

Research on scheduling and response-time analysis of real-time multiprocessor systems.

15/03/2023 – 01/10/2023 Pisa, Italy
POST-GRADUATE RESEARCHER TECIP, SCUOLA SUPERIORE SANT'ANNA

Scholarship for research on the topic: Analysis of real-time multiprocessor systems.

EDUCATION AND TRAINING

17/02/2023 Pisa, Italy
MASTER DEGREE IN EMBEDDED COMPUTING SYSTEMS Università di Pisa, Scuola Superiore Sant'Anna

Final grade 110/110 cum laude |

Thesis Scheduling and Response-Time Analysis of Parallel Real-Time Tasks for Symmetric Multicores

Link https://etd.adm.unipi.it/t/etd-01282023-143227/

2015 Pisa, Italy
BACHELOR DEGREE IN COMPUTER ENGINEERING Università di Pisa

Final grade 96/110 |

Thesis Analysis and testing of a smartwatch application for sleep monitoring and implementation of a preprocessing module in Java Android

2010 Livorno, Italy
DIPLOMA IN COMPUTER SCIENCE Istituto Tecnico Industriale Galileo Galilei

Final grade 90/100

LANGUAGE SKILLS

Mother tongue(s): **ITALIAN**

Other language(s):

	UNDERSTANDING		SPEAKING		WRITING
	Listening	Reading	Spoken production	Spoken interaction	
ENGLISH	C1	C1	B2	B2	B2

Levels: A1 and A2: Basic user; B1 and B2: Independent user; C1 and C2: Proficient user

DIGITAL SKILLS

Programmazione

Programmazione Python | Programmazione PHP | Conoscenza di linguaggi di programmazione C++ Java SQL LaTeX | JAVA, JAVASCRIPT, JSON | Programmazione HTML | Makefile | Fondamenti di CPLEX | CUDA C | conoscenze base di programmazione con MATLAB | Programmazione C++ | Programmazione C | Programmazione orientata agli oggetti, Programmazione concorrente, Programmazione Client-Server | Programmazione Java | Programmazione Javascript

Generali

AUTOSAR | Sistemi operativi Windows, Linux | Padronanza del Pacchetto Office (Word Excel PowerPoint ecc) | Utilizzo del broswer | Posta elettronica | Social Network

ADDITIONAL INFORMATION

DRIVING LICENCE

Driving Licence: A2

Driving Licence: B

PROJECTS

09/2022
Re-implement the BuildCore scripts using a Makefile Within the course of Component-Based Software Design of my master's degree, I developed this project in which I go to develop a particular makefile that goes to generate the initramfs that contain the minimum number of files needed to boot the system and a possible test application that represents a component to be used to start a virtual machine. Project developed on Ubuntu.

Tools: Makefile and Ubuntu

07/2022
Parallelization of an application As part of the Computer Architecture course of my master's degree, I developed this project where I had to parallelize the sequential code developed forcalculating the inverse of a matrix to evaluate the speedup obtained using parallel code.

Tools: CUDA c and c++

05/2022
Computation of the module of a complex number In the Digital System Design course of my master's degree, I developed this project in which I have to design a digital circuit for the calculation of the module of a complex number according to a certain approximate algorithm.

Tools: VHDL and Vivado

02/2021
Manipulator for pick and place purpose In the course of Robotics and Human-Machine interface of my master's degree, I developed this project in which I designed a redundant manipulator that was meant to move objects from one point to another. Starting from the description of the various links of the manipulator, continuing with the planning of a trajectory between the two points and then going to analyze the latter.

Tools: Robotic toolbox and Matlab

02/2020

Convolutional Neural Network for Medical Imaging Analysis As part of the Computational Intelligence course of my master's degree, I developed this project in which I went to develop this Convolutional Neural Network to perform the classification of abnormalities in mammography.

Tools: Google Colab and TensorFlow

PUBLICATIONS

Partitioned Fixed-Priority Scheduling of DAG Gang Tasks

Submitted at **IEEE Transactions on Computers**

Abstract:
The study of parallel task models for real-time systems has become fundamental due to the increasing computational demand of modern applications. Recently, gang scheduling has gained attention for improving performance in tightly synchronized parallel applications. Nevertheless, existing studies often overestimate computational demand by assuming a constant number of cores for each task. In contrast, the bundled model accurately represents internal parallelism by means of a string of segments demanding for a variable number of cores. This model is particularly relevant to modern real-time systems, as it allows transforming general parallel tasks into bundled tasks while preserving accurate parallelism. However, it has only been analyzed for global scheduling, which carries analytical pessimism and considerable run-time overheads. This paper introduces two response-time analysis techniques for parallel real-time tasks under partitioned, fixed-priority gang scheduling under the bundled model, together with a set of specialized allocation heuristics. Experimental results compare the proposed methods against state-of-the-art approaches.

IEEE Transactions on Computers

Scheduling and Response-Time Analysis of Parallel Real-Time Tasks for Symmetric Multicores – 2023

Accepted to be presented at Italian Workshop on Embedded Systems **(IWES 2023)**

Abstract:
The study of parallel task models for real-time systems has become fundamental due to the increasing computational demand of modern applications, which are executed in parallel to leverage the availability of multiple cores of multicore computing platforms and to boost performance.
In this context, the gang scheduling paradigm is receiving increasing attention thanks to the performance improvements it can provide for tightly-synchronized parallel applications. Existing works on real-time gang partitioned scheduling use a rigid model, where the number of cores required by a task is assumed to be constant, thus overestimating its computational demand. On the other hand, the bundled model, where tasks consist of segments (or bundles), each requiring a different number of cores, was introduced to obtain a more accurate representation of the tasks' parallelism. However, this model has only been analyzed for global scheduling, which is notably considered less predictable from the perspective of timing. To fill this gap, this work presents an analysis method for parallel real-time tasks under fixed-priority partitioned scheduling as well as the gang scheduling paradigms.
In particular, two schedulability analysis methods are proposed, one based on a closed-form formulation and the other based on an optimization technique. In addition, specialized partitioning heuristics are introduced. Finally, the results of an experimental evaluation are presented, comparing the proposed methods and considering different allocation heuristics.
